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(54) Self-aligned field effect transistor integrated circuit structure and method for making.

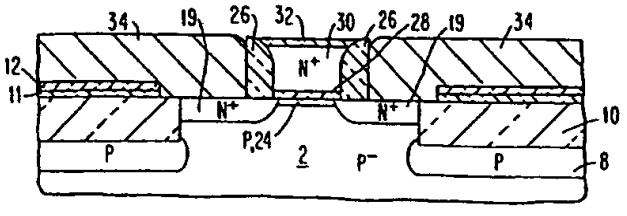
(57) A planar self-aligned field effect transistor integrated circuit structure comprising a patttern of narrow dimensioned dielectric regions (26) on a body (2), and a gate dielectric layer (28) on said body, and between certain of said dielectric regions (26).

PN junction regions (19) within said body (2) and in close proximity to and associated with the channel under said gate dielectric layer (28) form drain and source of the field effect transistors.

Doped polycrystalline silicon gate electrodes (30) on the surface of said gate dielectric layer (28) are arranged between certain of said narrow dimensioned regions (26).

Metal electrical contacts (34) to source and drain regions (19) fill the spaces between the remaining narrow dimensioned regions (26). The contacts (34) are self-aligned to said narrow dimensioned regions (26) and substantially planar with the tops of said regions.

FIG. 11



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graphy", published in the "Computer", Vol. 9, No. 2, February 1976, pp. 31 through 37. In that publication the substantial equipment costs and complexities of X-ray and electron beam lithography are described.

There have been alternative efforts to obtain narrow line widths and separations in the range of one micrometer or less by extending standard photolithography techniques and avoiding the need for the more expensive and complex techniques, such as electron beam or X-ray lithography. One such technique is described by H. B. Pogge in IBM Technical Disclosure Bulletin, November 1976, Vol. No. 6, entitled "Narrow Line Widths Masking Method". This method involves the use of a porous silicon followed by oxidation of porous silicon. Another technique is described by S. A. Abbas, et al, IBM Technical Disclosure Bulletin Vol. 20, No. 4, September 1977, pp. 1376 through 1378. This TDB describes the use of polycrystalline silicon masking layers which are made into masks by first using an intermediate mask of oxidation blocking material, such as silicon nitride in the formation of the polycrystalline silicon. Line dimensions below about two micrometers may be obtained by this technique. T. N. Jackson, et al, described "A Novel Sub-micron Fabrication Technique" in the March 1980 publication "Semiconductor International", pp. 77 through 83. This method for producing submicron line widths and devices does not require electron beam lithography but used a selective edge plating technique. The U.K. Patent 2,003,660 published March 14, 1979 describes a method for depositing an area of metal, for example metal on a substrate and forming narrow metal stripes by using a unidirectional plasma etching technique. K. H. Nicholas, U.S. 4,083,098 describes a method of making a plurality of closely spaced, but air isolated, conductive layers on an insulated substrate. He suggests no ohmic connections to the silicon body under the insulator supporting his conductive layers. The above

doped polycrystalline silicon as conductive layers such as shown in R. C. Wang, U.S. 3,750,268, issued August 7, 1973 and R. T. Simko, et al U.S. 3,984,822, issued October 5, 1976. However, as the density of devices has increased, there still remain problems involving isolation between devices, conductivity particularly at the first level of metallurgy contacting the semiconductor devices, and alignment of the levels of metallurgy to the device elements in the semiconductor integrated circuit.

In the usual methods for forming double polycrystalline silicon multilayer structures, silicon dioxide is used as the insulator between the layers. The silicon dioxide thickness between two polycrystalline layers is normally directly related to the thickness of the silicon gate oxide where a FET type device is being made. The usual thermal oxidation techniques are used to form the silicon dioxide layer.

The invention as claimed solves the problem of how to design and form an insulator of any desired thickness between the conductive layers, which are polycrystalline silicon for the gate electrodes and metal for other purposes, and, in particular, on the vertical regions between the layers of conductive material which are the electrical contacts to elements of field effect transistor integrated circuits.

The method for forming FET integrated circuits having a pattern of narrow dimensioned dielectric regions on the body of a monocrystalline semiconductor, preferably silicon, involves providing the silicon body and forming a first insulating layer on a major surface of the body. A highly doped polycrystalline silicon layer and a silicon nitride layer are then successively formed on the first insulating layer. Openings in the silicon nitride and polycrystalline

removed in areas away from the FET areas. A conductive layer of one or more wide variety of possible materials is now is now deposited using a lift-off mask upon the narrow dimensioned regions and on the silicon body to make contact to source/drain PN regions. Where the conductive layer is formed upon bare silicon, ohmic contacts can be formed thereto. A plastic material, such as a polyimide or photoresist, is deposited over this conductive layer to planarize the surface thereof. The structure is then placed in a reactive ion etching ambient where the conductive layer is uniformly etched together with the plastic layer until the tops of the narrow dimensioned regions are reached. The remaining plastic material is then removed to thereby form the substantially planar conductive layer with narrow dimensioned dielectric isolation separating portions of the conductive layer from other portions of the conductive layer and the polycrystalline silicon gate electrode.

The method can be used to form a variety of field effect transistor products. These structures are formed by appropriate modifications of the method described in the preceding paragraph to form suitable PN junctions, gate dielectric and electrode structures, PN contact regions, together with openings to the semiconductor body which have these elements formed therein. Logic and memory field effect transistor integrated circuits may be formed according to these methods to provide the beneficial results of high density with suitable conductivity of the metallurgy layers and good planarity, with its attendant yield and reliability.

The method may be adapted to form a short channel field effect transistor integrated circuit. This structure includes a silicon body having a pattern of narrow dimensioned dielectric regions on a major surface of said body. A gate dielectric layer is located on the major surface between certain portions of the narrow dimensioned regions.

used to form a very dense field effect transistor integrated circuit structure. A near-intrinsic P-substrate 2 having a resistivity of 20 to 100 ohm-cm is a preferred substrate for the process. P type substrate of monocrystalline silicon substrate having a 10-20 ohm-cm resistivity may alternatively be the basic foundation structure for the process. P+ substrates with low doped P epitaxy can also be utilized.

The first series of method steps involve the formation of isolation means for isolating regions of monocrystalline silicon from other regions of monocrystalline silicon in substrate 2. The isolation may preferably be partial dielectric isolation using materials such as silicon dioxide, glass, etc. The preferred pattern of partial dielectric isolation 10 define monocrystalline silicon surface regions wherein field effect devices will ultimately be formed. Underneath the dielectric isolation is a P ion implantation region 8 to prevent surface leakage at the interface between the substrate and the dielectric isolation. There are many ways in the art to form dielectric isolation regions of this type. It is preferred to use the processs described in the Magdo et al patent application serial number 150,609, filed June 7, 1971, or Peltzer U.S. Patent 3,648,129. Alternatively, the process described in the J. A. Bondur et al U.S. patent 4,104,086 can be used. In the above patent application and patents the processes for forming partial dielectric isolation regions 10 are described in detail. However, the process briefly involves forming silicon dioxide layer 4 on the silicon body 2. A layer of silicon nitride 6 is formed thereover. The layers 4, 6 are removed by conventional lithography in areas designated to have dielectric isolation. The silicon body 2 is etched using the remaining layers 4, 6 as a mask. P region 8 is formed by ion implantation using boron as the impurity to form the FIGURE 1 structure. The structure is placed in an oxidizing ambient until the silicon dioxide

too low, planarization and the breaking of the metal is more difficult to achieve. The polycrystalline silicon layer is doped N+ type either in situ during deposition of the polycrystalline silicon layer or through ion implantation of an N+ type impurity subsequent to deposition of the polycrystalline silicon layer. Phosphorus is a suitable impurity for this doping. The polycrystalline silicon layer makes contact to the silicon body 2 in areas void of the first insulating layer 11, 12. A silicon nitride layer 20 which may be, for example, about 50 nm in thickness is deposited by chemical vapor deposition according to the following conditions: by decomposing SiH_4 and N_2 at 800° to produce the FIGURE 4 structure. Other suitable insulating layers or combination of layers can be substituted for the silicon nitride.

Standard photolithography and etching techniques may be utilized to form openings in this silicon nitride layer 20 over the areas designated to be gate regions of the integrated circuit. Using this silicon nitride mask the structure is placed in a reactive ion or plasma etching environment for a polycrystalline silicon having typically the conditions as follows: for example, CF_4/Argon, Cl_2/Argon or CCl_4/Argon, SF_6 or $SF_6 + Cl_2$, RF parallel plate structure, about 10 microns pressure, 0.16 watts/cm^2 power density and 10cc/min. flow rate and using the apparatus described in the Harvilchuck, et al patent application serial number 594,413 filed July 9, 1975 and continuation patent application serial number 822,775 filed August 8, 1977. The reactive ion etching process is completed when it reaches the monocrystalline silicon body 2. The resulting structure has horizontal surfaces and vertical surfaces.

A conformal layer 26 is deposited on both the substantially horizontal surfaces and the substantially vertical surfaces

The structure of FIGURE 6 is now subjected to thermal oxidation ambient so as to form the silicon dioxide gate dielectric. The thickness of the gate dielectric may be between about 20 to 50 nm, and preferably is approximately 45 nm.

A second layer of N+ doped polycrystalline silicon 30 is formed by a procedure similar to that described above over the entire major surface of the structure, as shown in FIGURE 7. The N+ doping may be done in situ or by phosphorus ion implantation following the polycrystalline silicon deposition. A photoresist or polyimide layer 31 is blanket deposited over the N+ polycrystalline silicon layer 30. The structure is placed in a reactive ion etching ambient which has a similar etch rate between the photoresist 31 chosen and the N+ polycrystalline silicon 30. The blanket reactive ion etching continues until the silicon nitride layer 20 is reached leaving the polycrystalline silicon 30 only in the designated gate electrode areas, as shown in FIGURE 8. After forming patterns in polycrystalline silicon 30, silicon dioxide layer 32 of approximately 40 nm in thickness is grown on the surface of the second polycrystalline silicon gate electrode areas 30 to produce the structure of FIGURE 8. The silicon nitride layer 20 is removed by hot phosphoric acid H_3PO_4. The structure is placed in a reactive ion etching ambient for polycrystalline silicon to remove the remaining first polycrystalline silicon layer 18 and to produce the structure shown in FIGURE 9. Using a non-critical mask, portions of the silicon dioxide 32 and 26 are removed in areas away from the FET areas.

Using a suitable lift-off mask, a metal layer 34 is deposited over the narrow dimensioned dielectric regions 26, gate electrode regions 30, 32 and areas therebetween so that in the areas between the narrow dimensioned dielectric

percent coverage of diffusions and gate regions is obtained. FIGURE 12 shows a metal pattern contacting the N+ polycrystalline silicon pattern 30 at its sides. The metal contact is done in a region where the silicon dioxide layer 32 covering the polycrystalline silicon pattern 30 was removed earlier using a non-critical mask. Alternatively, the polycrystalline silicon patterns 32 can be contacted by a higher level metallization pattern through a contact hole in silicon dioxide 32.

Referring now more particularly to FIGURES 13 through 20, a second method embodiment is described. The process for forming the recessed dielectric isolation 10 on the surface regions of intrinsic silicon substrate 2 to isolate monocrystalline silicon regions designated to be sites for field effect transistor devices is formed according to the procedures described in relation to the FIGURE 1 through FIGURE 12 embodiment. Like numbers are indicative of like structures to the FIGURE 1 through FIGURE 12 embodiment.

A first insulating layer of silicon nitride 12 is deposited by chemical vapor deposition as described above. The thickness of the layer may be about 150 nm. Conventional lithography and etching is utilized to pattern the silicon nitride layer 12 so as to open all active device areas, as shown in FIGURE 13. A silicon dioxide mask layer 44 is formed on the surface of the active semiconductor area by means of chemical vapor deposition of silicon dioxide followed by standard lithography and etching techniques to form the silicon dioxide mask 44, as shown in the FIGURE 13. The preferred etching is by reactive ion etching to produce the substantially vertical sidewalls of the mask 44. The exposed silicon body 2 serves as the end point detector.

Referring now to FIGURE 14, the process continues by reactive ion etching the silicon body 2 using the mask 44 in a

heat cycle to produce the structure of FIGURE 15.

The mask 44 is removed by a suitable dipped chemical etching process. A conformal layer of silicon dioxide 22 of about 1 micrometer in thickness is deposited over the structure by a standard chemical vapor deposition process as described above. The structure is then put in a directional reactive ion etching ambient which acts to remove the horizontal layer of the first conformal insulating silicon dioxide coating 22 and to provide narrow openings to the exposed surface of the monocrystalline silicon surface region of body 2 between the vertical surfaces of the insulating coating. An ion implantation of a suitable dosage of boron at low energy is made to obtain the P "short-channel" region 24 at the exposed silicon surface, as shown in FIGURE 16.

The silicon dioxide mask 22 is removed by standard dipped chemical etching to obtain the structure of FIGURE 17. A second conformal coating 26 is deposited on both the substantially vertical and substantially horizontal surfaces. The thickness of the coating may be of the order of 0.5 micrometers. Directional reactive ion etching is now utilized to substantially remove the horizontal layer and to provide a pattern of narrow dimensioned dielectric regions 26 on the silicon body to produce the structure shown in FIGURE 18.

The exposed surface of the monocrystalline silicon body 2 is thermally oxidized between certain of the narrow dimensioned regions to form the gate dielectric regions 28 for the integrated circuit. The gate dielectric oxide is preferably about 40 nm in thickness. A second layer of N+ doped polycrystalline silicon 30 is deposited by chemical vapor deposition as described above. Also as described above, the N+ doping may be incorporated into the polycrystalline

semiconductor, the field effect transistor of FIGURE 20 is bilateral or symmetrical, in that the source and drain can interchange their roles readily during circuit operation. The overlap capacitance of the gate electrode over the source/drain is near zero. The parasitic capacitance of the source/drain to substrate is diminished by the introduction of the dielectric layer of silicon dioxide 46. The only region for this tiny capacitance is the approximately 0.6 micrometer lateral N+ diffusion 19.

4. Method for forming the structure as claimed in claims 1 to 3,
characterized by providing a silicon body (2); forming a highly doped first polycrystalline silicon layer (18) contiguous to said body in designated active device areas and dielectrically isolated from said body in other areas; forming a silicon nitride insulating layer (20) above the said polycrystalline silicon layer (18); forming openings in said silicon nitride layer (20) and said polycrystalline silicon layer (18) by reactive ion etching in the areas designated to be the gate regions of said integrated circuits which results in the structure having substantially horizontal surfaces and substantially vertical surfaces with the surface of said silicon body exposed in the designated gate areas; outdiffusing using a heat cycle the said dopant from said polycrystalline silicon layer (18) into said body (2) to form the source/drain regions (19) for said field effect integrated circuit; forming a conformal insulating layer on both said substantially horizontal surfaces and said substantially vertical surfaces; reactive ion etching said conformal insulating layer to substantially remove said conformal layer from said horizontal surfaces, both from above the said polycrystalline silicon layer (18) and said surface of the silicon body (2) exposed in the designated gate areas, and to provide said narrow dimensioned dielectric regions (26) on said silicon body (2); thermally oxidizing said surface of the silicon body exposed between certain of said narrow dimensioned regions to form the gate dielectric regions (28) for the said integrated circuits; forming a highly doped second polycrystalline silicon layer (30) on the designated said gate dielectric regions (28) for said field effect transistor integrated circuits wherein said layer is the gate electrode for said circuits; removing the remaining

monocrystalline silicon to form PN source/drain regions (19) therein; etching away said silicon dioxide mask (44) to provide substantially vertical and substantially horizontal surfaces on the structure and with openings to the surface of said monocrystalline silicon regions; depositing a first conformal insulating coating (22) on both said substantially vertical and substantially horizontal surfaces; reactive ion etching said first conformal insulating coating to substantially remove said first conformal coating from said horizontal surfaces and to provide narrowed said openings therebetween due to presence of said insulating coating on the vertical surfaces of said monocrystalline silicon regions; forming a short-channel region (24) through said narrowed openings; etching away said first conformal insulating coating (22) on the vertical surfaces; depositing a second conformal insulating coating (26) on both said substantially vertical and substantially horizontal surfaces; reactive ion etching said second conformal coating (26) to substantially remove said second conformal coating from said horizontal surfaces and to provide narrow dimensioned dielectric regions (26) on said silicon body; thermally oxidizing the surface of said monocrystalline silicon between certain of said narrow dimensioned regions (26) to form the gate dielectric regions (28) for said integrated circuit; forming a highly doped second polycrystalline silicon layer (30) on the designated said gate dielectric regions (28) for said field effect transistor integrated circuits wherein said layer is the gate electrode for said circuits; removing the remaining said first polycrystalline silicon layer (18) by reactive ion etching to leave the said narrow dimensioned regions (26) and said second polycrystalline silicon layer (30) on said gate dielectric (28) on said

surface of said second polycrystalline silicon layer (30) are removed so that portions of said conductive layer (34) can make electrical contact to said gate electrode.

10. Method of one or several of the claims 4 to 9, characterized in that the said forming a conductive layer includes depositing a layer (34) of aluminum over said narrow dimensioned regions (26) and areas in between, blanket depositing a plastic material (35) over the said aluminum layer (34) to planarize the surface, reactive ion etching the said plastic material (35) and said aluminum layer (34) until the tops of said narrow dimensioned regions (26) are reached and removing the remaining said plastic material (35).

11. Method of one or several of the claims 4 to 10, characterized in that said polycrystalline gate electrode (30) is electrically contacted on its edge by a conductive layer of the same material and formed at the same time as said conductive layer (34) for contacting said source/drain regions (19).

12. Method of one or several of the claims 4 to 10, characterized in that said polycrystalline silicon gate elctrode (30) is electrically contacted by a higher level metal electrical contact from above.

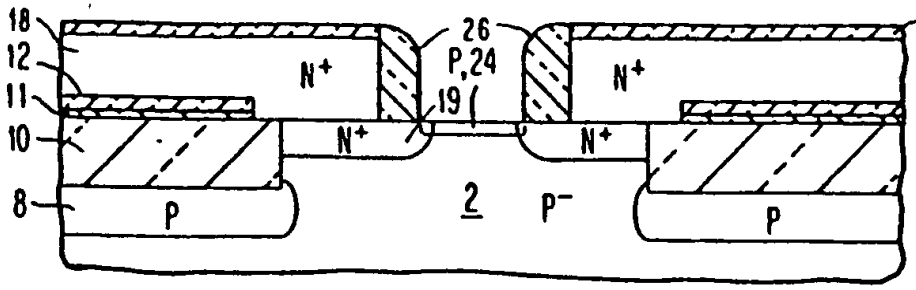

FIG.6

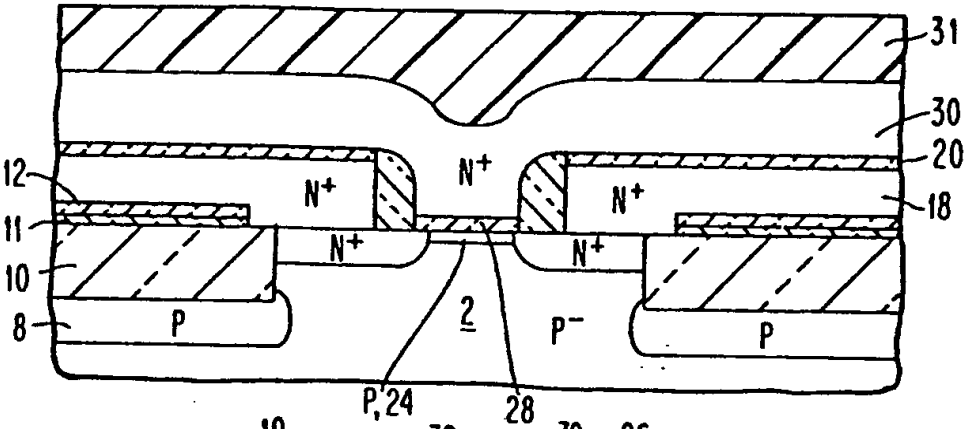

FIG.7

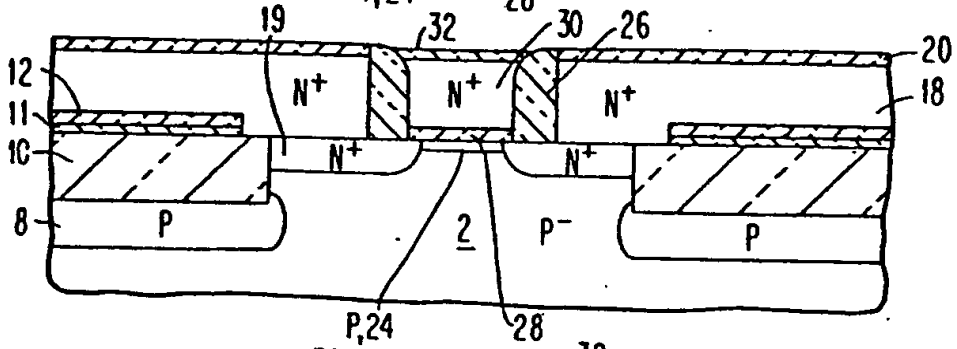

FIG.8

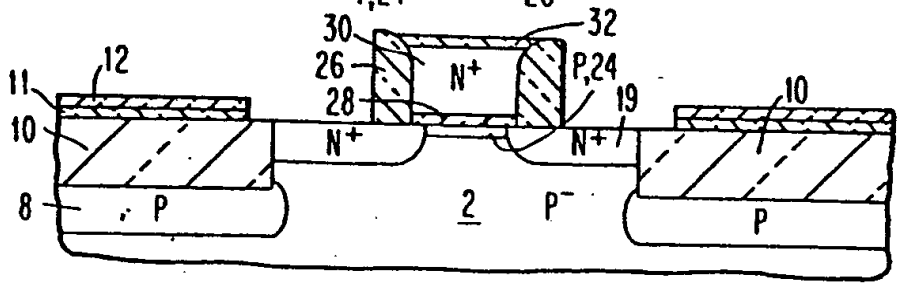

FIG.9

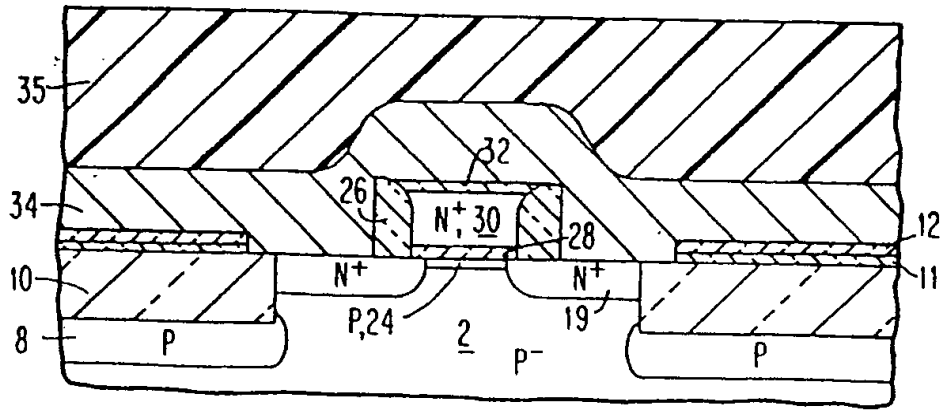

FIG.10

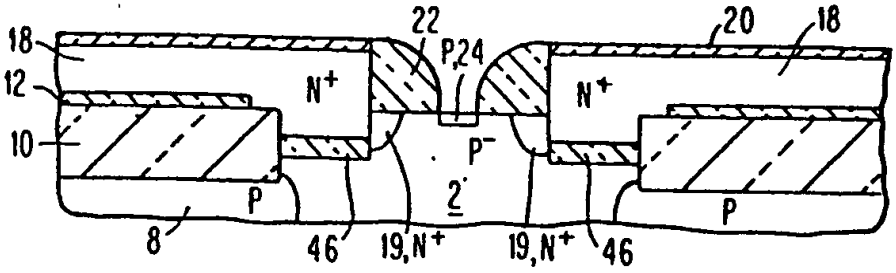

FIG.16

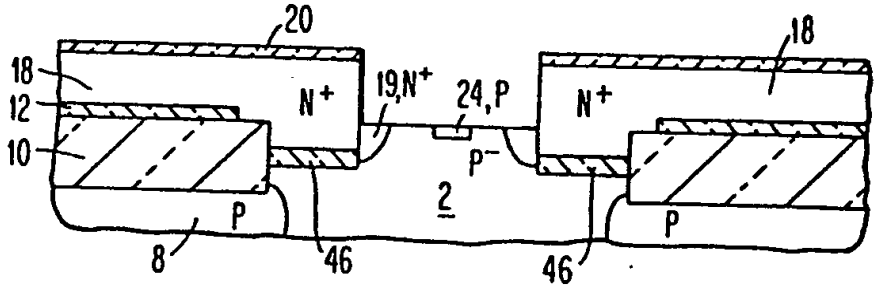

FIG.17

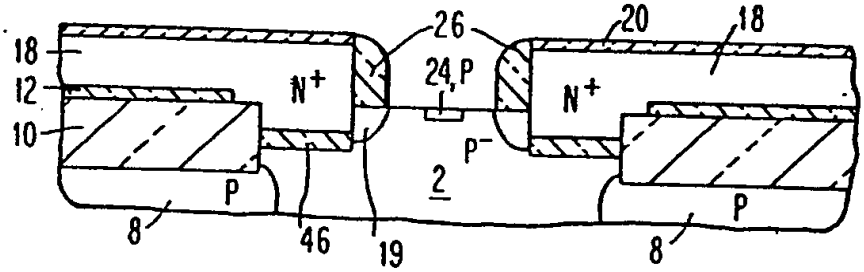

FIG.18

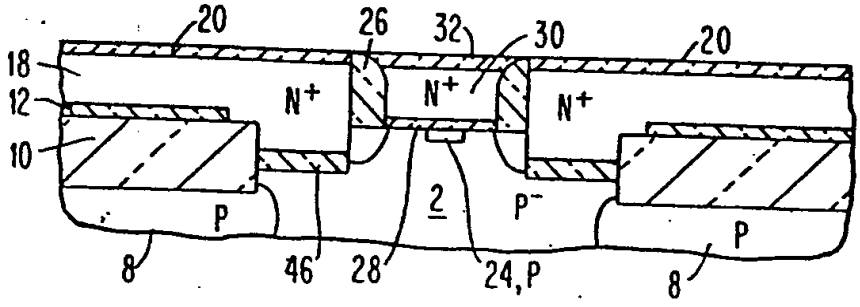

FIG.19

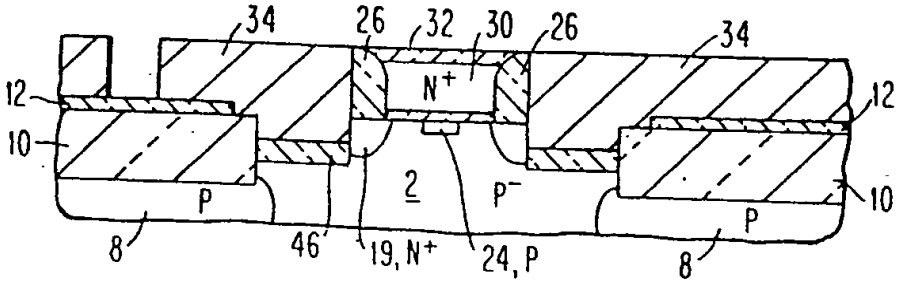

FIG. 20

AUSTRALIAN PATENT OFFICE

WRITTEN OPINION

	Date of mailing *day/month/year* 20 FEB 2003
Applicant's or agent's file reference 552689SG:SDB:IRG	**REPLY DUE** within FIVE MONTHS of the date of the Registrar's letter enclosing the written opinion

Application No.	Application Filing Date *(day/month/year)*	Priority Date *(day/month/year)*
SG 200102828-1	12 May 2001	15 May 2000

International Patent Classification (IPC) (as indicated in the search report)

Int. Cl.[7] H01L 21/336, 29/78, 29/786

Applicant

INTERNATIONAL BUSINESS MACHINES CORPORATION

1. This First written opinion consists of a total of 4 sheets.
2. This opinion contains indications relating to the following items:.

I	[X]	Basis of the opinion
II	[ ]	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
III	[ ]	Lack of unity of invention
IV	[X]	Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
V	[ ]	Certain documents cited
VI	[ ]	Certain defects in the application
VII	[X]	Certain observations on the application

3. This opinion is based upon the assumption that the priority claim is valid.
4. The search report used was issued by the **Australian Patent Office**, and the date of completion is: **14 February 2003**
5. If no reply is filed, the examination report will be established on the basis of this opinion.
6. The date by which the examination report will be established is: **15 August 2004**

Name and mailing address	Authorized Officer
AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile no. 61 2 62853929	**F.C.PEARSON**

AUSTRALIAN PATENT OFFICE

WRITTEN OPINION

Application No.
SG 200102828-1

I. Basis of the opinion

1. This opinion has been drawn on the basis of:

[X] the application as originally filed.

[ ] the description, pages , as originally filed,
pages , filed with the request,
pages , received on with the letter of

[ ] the claims, pages , as originally filed,
pages , filed with the request,
pages , received on with the letter of

[ ] the drawings, sheets/fig. , as originally filed,
sheets/fig. , filed with the request,
sheets/fig. , received on with the letters of

[ ] the sequence listing part of the description:
pages , as originally filed
pages , filed with the demand
pages , received on with the letter of

2. The amendments have resulted in the cancellation of: pages:
sheets of drawings/figures No :

3 [ ] This opinion has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box.

4. Additional observations, if necessary:

AUSTRALIAN PATENT OFFICE

WRITTEN OPINION

Application No.
SG 200102828-1

IV. Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims **1-10, 12-32, 34-38, 40-43**	YES
	Claims **11, 33, 39**	NO
Inventive step (IS)	Claims **1-10, 12-32, 34-38, 40-43**	YES
	Claims **11, 33, 39**	NO
Industrial applicability (IA)	Claims **1-43**	YES
	Claims	NO

2. Citations and explanations

Novelty (N) and Inventive Step (IS):

The independent claims are claims 1, 11, 21, 33. The invention relates to manufacturing the two gate electrodes of a dual gate MOSFET independently so that the gates can be electrically separated and made of different materials and thicknesses and so on. The independent claims are directed to various aspects of this concept and are therefore directed to the same invention.

Claims 11, 33 and 39 are disclosed in US patent 5818070. This shows a thin film transistor with two gates made independently and of different materials. Therefore claims 11, 33 and 39 are not novel and not inventive.

The remaining claims appear to be novel and inventive. The citations US 5818070 (column 13 lines 9-12) and US 5296727 (column 5 line4-5), for examples, indicate that the two gates are normally electrically connected. Therefore the feature of electrically separating the gates seems to be novel and inventive.

The invention clearly has industrial applicability.

AUSTRALIAN PATENT OFFICE

WRITTEN OPINION

Application No.

SG 200102828-1

VII. Certain observations on the application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

1. The title, the "field of invention" at page 1 and the description as a whole are directed to a "self-aligned double gate MOSFET". However the claims are directed merely to a transistor. Therefore the claims do not define the invention and are not fairly based.

2. Claim 33 does not define the invention since it does not state that the two gate electrodes are "above" and "below" each other. See for example page 1 paragraph 1, "top and bottom gates".

[X] The claimed invention is patentable according to Section 13(2); or

[ ] The claimed invention is unpatentable according to Section 13(2) because:

AUSTRALIAN PATENT OFFICE

SEARCH REPORT

Applicant's or agent's file reference 552689SG:SDB:IRG		
Application No. SG 200102828-1	Application Filing Date *(day/month/year)* 12 May 2001	(Earliest) Priority Date *(day/month/year)* 15 May 2000
Applicant INTERNATIONAL BUSINESS MACHINES CORPORATION		

This search report consists of a total of 4 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. [ ] **Certain claims were found unsearchable** (See Box I)

2. [ ] **Unity of invention is lacking** (See Box II)

3. [ ] The application contains disclosure of a **nucleotide and/or amino acid sequence listing** and the search was carried out on the basis of the sequence listing

   [ ] filed with the application

   [ ] furnished by the applicant separately from the application,

   [ ] but not accompanied by a statement to the effect that it did not include matter going beyond the disclosure in application as filed

4. With regard to the **title,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established by this Office to read as follows:

5. With regard to the **abstract,**

   [X] the text is approved as submitted by the applicant

   [ ] the text has been established by this Office as it appears in Box III

6. The figure of the **drawings** to be published with the abstract is Figure No. 49

   [X] as suggested by the applicant.

   [ ] because the applicant failed to suggest a figure

   [ ] because this figure better characterises the invention

   [ ] None of the figures

AUSTRALIAN PATENT OFFICE

SEARCH REPORT

Application No.
SG 200102828-1

A. CLASSIFICATION OF SUBJECT MATTER

According to International Patent Classification (IPC)

Int. Cl. [7] H01L 21/336, 29/78, 29/786

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the search (name of data base and, where practicable, search terms used)

DWPI JAPIO: ic class H01L, fet, mosfet, field-effect, unipolar, second, two, dual, double, multiple, plural, several, gate, above, below, top, bottom, on, beneath, over, under, channel, self-align

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5818070 A (YAMAZAKI et al) 6 October 1998. See claims 8 and 9.	11-20, 33-43
A	See claim 1 lines 16-19.	
A	US 6037204 A (CHANG et al) 14 March 2000. See column 4 lines 37-47.	
A	US 5646058 A (TAUR et al) 8 July 1997. See abstract.	

[X] Further documents are listed in the continuation of Box C

[X] See patent family annex

* Special categories of cited documents:

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Date of submission of the request to the Australian Patent Office	Date of completion of the search report	Date of mailing of the search report
14 October 2002	14 February 2003	20 FEB 2003

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SEARCH REPORT

Application No.
SG 200102828-1

C (Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5296727 A (KAWAI et al) 22 March 1994. See abstract and column 5 lines 1-5.	
A	EP 043944 B1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 8 October 1986. See whole document.	

AUSTRALIAN PATENT OFFICE

SEARCH REPORT

PATENT FAMILY MEMBERS

Application No.
SG 200102828-1

Patent Document Cited in Search Report		Patent Family Member					
US	5818070	US	5644147	JP	8023100		
US	6037204	NONE					
US	5646058	JP	8046212	US	5604368		
US	5296727	JP	5013438				
EP	0043944	US	4488162	US	4471522	US	4378627
		JP	57032674				END OF ANNEX